the present invention also advantageously provide FETs having a gate oxide layer. The gate oxide layer advantageously reduces gate leakage current and increases the drain current.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

What is claimed is:

1. A field effect transistor comprising:

a first semiconductor layer of a first conductivity type;

a first dielectric layer disposed upon said first semiconductor layer;

a second semiconductor layer of a second conductivity type disposed upon said first dielectric layer wherein said first semiconductor layer and said second semiconductor layer are disposed on two opposite surfaces of said first dielectric layer;

a second dielectric layer disposed upon said second semiconductor layer wherein said first dielectric layer and said second dielectric layer are disposed on two opposite surfaces of said second semiconductor layer; and

a third semiconductor layer of said first conductivity type disposed upon said first semiconductor layer, wherein a first portion of the third semiconductor layer of said first conductivity type is between a first and a second portion of said first dielectric layer, a second portion of the third semiconductor layer of said first conductivity type is between a first and a second portion of said second semiconductor layer and a third portion of the third semiconductor layer of said first conductivity type is between a first and a second portion of said second dielectric layer.

2. The field effect transistor according to claim **1**, wherein said third semiconductor layer comprises:

a first portion, having a heavy doping concentration, disposed proximate said second dielectric layer; and

a second portion, having a moderate doping concentration, disposed proximate said second semiconductor layer said first dielectric layer and said first semiconductor layer.

3. The field effect transistor according to claim **1**, wherein:

said first semiconductor layer comprises a heavily n-doped semiconductor;

said second semiconductor layer comprises a heavily p-doped semiconductor; and

said third semiconductor layer comprises a moderately n-doped semiconductor.

4. The field effect transistor according to claim **1**, wherein:

said first semiconductor layer further comprises a heavily p-doped semiconductor;

said second semiconductor layer further comprises a heavily n-doped semiconductor;

and

said third semiconductor layer further comprises a moderately p-doped semiconductor.

5. The field effect transistor according to claim **1**, wherein said third semiconductor layer comprises a strained semiconductor layer.

6. The field effect transistor according to claim **1**, wherein said third semiconductor layer partially extends into said first semiconductor layer.

7. The field effect transistor according to claim **1**, further comprising a third dielectric layer disposed between said third semiconductor layer and said first and second portions of said second semiconductor layer.

8. The field effect transistor according to claim **1** further comprising a third dielectric layer disposed between said third semiconductor layer and said first and second portion of said second dielectric layer, said first and second portions of said second semiconductor layer and said first and second portions of the first dielectric layer.

9. A field effect transistor comprising:

a first semiconductor layer comprising a first portion of a first conductivity type;

a first dielectric layer disposed upon said first semiconductor layer;

a second semiconductor layer comprising a first and second portion of a second conductivity type, wherein said second semiconductor layer is disposed upon said first dielectric layer;

a second dielectric layer disposed upon said second semiconductor layer;

a third semiconductor layer of a first conductivity type disposed upon said first portion of said first semiconductor layer, wherein a first portion of the third semiconductor layer of said first conductivity type is between a first and a second portion of said first dielectric layer, a second portion of the third semiconductor layer of said first conductivity type is between said first and second portions of said second semiconductor layer and a third portion of the third semiconductor layer of said first conductivity type is between a first and a second portion of said second dielectric layer; and

a third dielectric layer disposed between said third semiconductor layer and said first and second portions of said second semiconductor layer.

10. The field effect transistor according to claim **9**, wherein:

said first portion of said first semiconductor layer comprises a heavily n-doped semiconductor; and

said first and second portions of said second semiconductor layer comprise a heavily p-doped semiconductor; and further comprising;

a first portion of said third semiconductor layer proximate said second semiconductor layer comprises a moderately n-doped semiconductor; and

a second portion of said third semiconductor layer proximate said second dielectric layer comprises a heavily n-doped semiconductor.

11. The field effect transistor according to claim **9**, wherein:

said first semiconductor layer further comprises a second portion of said second conductivity type; and

said second semiconductor layer further comprises a third and fourth portion of said first conductivity type; and further comprising;

a fourth semiconductor layer of said second conductivity type disposed upon said second portion of said first semiconductor layer between a third and a fourth portion of said first dielectric layer, said third and said fourth portions of said second semiconductor layer and a third and a fourth portion of said second dielectric layer; and

a fourth dielectric layer disposed between said fourth semiconductor layer and said third and said fourth portions of said second semiconductor layer.